In The Claims:

1. (currently amended) A frequency synthesizing circuit, the circuit being digital, comprising:

a multiplexor having at least a first input, a second input, an output, and a control terminal;

a controller having at least an input and an output, wherein the output coupling to the control terminal of the multiplexor provides at least one-bit signal to select either data feeding the first input or data feeding the second input of the multiplexor to pass the multiplexor;

a first memory device coupling to the first input of the multiplexor for storing a first reference frequency sampled from sinusoidal waves;

a second memory device coupling to the second input of the multiplexor for storing a second reference frequency sampled from sinusoidal waves;

a linear feedback shift register coupling to the input of the controller, wherein the linear feedback shift register stores a target frequency so as to compare with a predetermined threshold in sequence; and

a digital clock signal for clocking a sequential operation of the frequency synthesizing circuit.

2. (currently amended) The sequential operation of a frequency synthesizing circuit, the frequency synthesizing circuit ~~as recited in claim 1;~~ being digital and comprising:

a multiplexor having at least a first input, a second input, an output, and a control terminal;

a controller having at least an input and an output, wherein the output coupling to the control terminal of the multiplexor provides at least one-bit signal to select either data feeding the first input or data feeding the second input of the multiplexor to pass the multiplexor;

a first memory device coupling to the first input of the multiplexor for storing a first reference frequency;

a second memory device coupling to the second input of the multiplexor for storing a second reference frequency;

a linear feedback shift register coupling to the input of the controller, wherein the linear feedback shift register stores a target frequency so as to compare with a predetermined threshold in sequence; and

a digital clock signal for clocking a sequential operation of the frequency synthesizing circuit;

wherein

the target frequency is compared with the predetermined threshold for determining either data feeding the first input of the multiplexor or data feeding the second input of the multiplexor to pass to the output of the multiplexor depending on the target frequency being larger or smaller than the predetermined threshold, and

the target frequency is shifted by one position for next comparison until a minimal resolution does not distinguish a difference between the target frequency and the predetermined threshold.

Claims 3-4. (canceled)

5. (original) The minimal resolution of the frequency synthesizing circuit as recited in claim 2, wherein the minimal resolution is determined by a ratio of a difference between the first reference frequency and the second reference frequency to a two's power, the power is the order of the linear feedback shift register.

6. (currently amended) A frequency synthesizing system, comprising:

a multiplexor having at least a first input, a second input in parallel, an output, and a control terminal;

a controller having at least an input and an output, wherein the output coupling to the control terminal of the multiplexor provides at least one-bit signal to select either data feeding the first input or data feeding the second input of the multiplexor to pass;

a first memory device coupling to the first input of the multiplexor for storing transformation of a first reference frequency, wherein the transformation is sinusoidal function;

a second memory device coupling to the second input of the multiplexor for storing

transformation of a second reference frequency, wherein the transformation is sinusoidal function;

a linear feedback shift register coupling to the input of the controller, wherein the linear feedback shift register stores a target frequency so as to compare with a predetermined threshold in sequence; and

a digital clock signal for clocking a sequential operation of the frequency synthesizing system.

7. (currently amended) The sequential operation of a frequency synthesizing system, the frequency synthesizing system ~~as recited in claim 6;~~ comprising:

a multiplexor having at least a first input, a second input in parallel, an output, and a control terminal;

a controller having at least an input and an output, wherein the output coupling to the control terminal of the multiplexor provides at least one-bit signal to select either data feeding the first input or data feeding the second input of the multiplexor to pass;

a first memory device coupling to the first input of the multiplexor for storing transformation of a first reference frequency;

a second memory device coupling to the second input of the multiplexor for storing transformation of a second reference frequency;

a linear feedback shift register coupling to the input of the controller, wherein the linear feedback shift register stores a target frequency so as to compare with a predetermined threshold in sequence; and

a digital clock signal for clocking a sequential operation of the frequency synthesizing system;

wherein

the target frequency compared with the predetermined threshold for determining either data feeding the first input of the multiplexor or the second input of the multiplexor to pass to the output of the multiplexor depending on the target frequency being larger or smaller than the predetermined threshold, and

the target frequency is shifted by one position for next comparison until a minimal resolution does not distinguish a difference between the target frequency and the predetermined threshold.

Claim 8-9. (canceled)

10. (original) The minimal resolution of the frequency synthesizing system as recited in claim 7, wherein the minimal resolution is determined by a ratio of a difference between the first reference frequency and the second reference frequency to two to the power of the order of the linear feedback shift register.

11. (new) A frequency synthesizing circuit, the circuit being digital, comprising:

a multiplexor having at least a first input, a second input, an output, and a control terminal;

a controller having at least an input and an output, wherein the output coupling to the control terminal of the multiplexor provides at least one-bit signal to select either data feeding the first input or data feeding the second input of the multiplexor to pass the multiplexor;

a first memory device coupling to the first input of the multiplexor for storing a first reference frequency;

a second memory device coupling to the second input of the multiplexor for storing a second reference frequency;

a linear feedback shift register coupling to the input of the controller, wherein the linear feedback shift register stores a target frequency so as to compare with a predetermined threshold in sequence, and an order of the linear feedback shift register determines the minimal resolution; and

a digital clock signal for clocking a sequential operation of the frequency synthesizing circuit.

12. (new) A frequency synthesizing system, comprising:

a multiplexor having at least a first input, a second input in parallel, an output, and a control terminal;

a controller having at least an input and an output, wherein the output coupling to the control terminal of the multiplexor provides at least one-bit signal to select either data feeding the first input or data feeding the second input of the multiplexor to pass;

a first memory device coupling to the first input of the multiplexor for storing transformation of a first reference frequency;

a second memory device coupling to the second input of the multiplexor for storing transformation of a second reference frequency;

a linear feedback shift register coupling to the input of the controller, wherein the linear feedback shift register stores a target frequency so as to compare with a predetermined threshold in sequence, and an order of the linear feedback shift register determines an order of the minimal resolution; and

a digital clock signal for clocking a sequential operation of the frequency synthesizing system.